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ARTICLE

# $MoS_2$ Memristors Exhibiting Variable Switching Characteristics toward Biorealistic Synaptic Emulation

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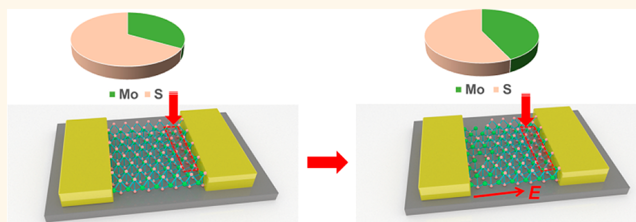
Supporting Information

**ABSTRACT:** **Memristors based on 2D layered materials could provide biorealistic ionic interactions and potentially enable construction of energy-efficient artificial neural networks capable of faithfully emulating neuronal interconnections in human brains. To build reliable 2D-material-based memristors suitable for constructing working neural networks, the memristive switching mechanisms in such memristors need to be systematically analyzed. Here, we present a study on the switching characteristics of the few-layer $MoS_2$ memristors made by mechanical printing. First, two types of dc-programmed switching characteristics, termed rectification-mediated and conductance-mediated behaviors, are observed among different $MoS_2$ memristors, which are attributed to the modulation of $MoS_2$/metal Schottky barriers and redistribution of vacancies, respectively. We also found that an as-fabricated $MoS_2$ memristor initially exhibits an analog pulse-programmed switching behavior, but it can be converted to a quasi-binary memristor with an abrupt switching behavior through an electrical stress process. Such a transition of switching characteristics is attributed to field-induced agglomeration of vacancies at $MoS_2$/metal interfaces. The additional Kelvin probe force microscopy, Auger electron spectroscopy analysis, and electronic characterization results support this hypothesis. Finally, we fabricated a testing device consisting of two adjacent $MoS_2$ memristors and demonstrated that these two memristors can be ionically coupled to each other. This device interconnection scheme could be exploited to build neural networks for emulating ionic interactions among neurons. This work advances the device physics for understanding the memristive properties of 2D-material-based memristors and serves as a critical foundation for building biorealistic neuromorphic computing systems based on such memristors.**




**KEYWORDS:** *2D materials, $MoS_2$, nanoelectronics, memristors, memories, defects*

There has been rapid progress toward the realization of artificial intelligence (AI) systems. Especially, artificial neural networks, the electronic mimic of human brains, could enable the creation of AI systems with high-performance analyzing and computing capabilities. However, a human brain typically contains billions of neurons that are connected to one another by trillions of contacts called synapses. Designing electronic devices that approach this level of connectivity and construct an artificial neural network capable of faithfully emulating complicated ionic neuronal interactions involved in brain functions remains a grand challenge. The current neural network systems constructed using conventional electronic components such as complementary metal−oxide−semiconductor (CMOS) devices need to be intensively programmed using software. This leads to a formidable computing complexity and extremely high (typically megawatt-level) power consumption. Such drawbacks severely hinder the practical application of such state-of-the-art neural-network systems for power-hungry computing tasks, such as multimedia streaming in remote clinical operations, virtual reality systems, and control of flexible aircrafts and robotic systems. To tackle these challenges, researchers are exploring alternative device architectures and principles to CMOS-based ones, as well as different ways for device interconnections. Such efforts aim at ultimately realizing energy-efficient neuromorphic computing processes at the hardware level. Emerging nanoelectronic devices known as memristors and memtransistors have become promising candidates for such an application. State-of-the-art memristors are made from transition-metal oxides.[1−5] In such an oxide-

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based memristor, external electrical stimulations (*e.g.*, dc voltages or voltage pulses) result in a programmable modulation of the oxide channel's electrical conductance, therefore forming a series of conductance states capable of emulating synaptic functions (*e.g.*, synaptic plasticity). Specifically, these conductance states are determined by the distribution of internal ions or ionic vacancies in the oxide channel, and the switching of the states is attributed to the formation and rupture of a conductive filament that connects the two electrodes sandwiching the oxide channel.[1,6] Networks of such memristors, in the form of crossbar structures, have been widely studied for neural network implementations.[7,8] However, the memristors in these networks lack an interaction mechanism, which is critical for faithfully emulating the interactions among biological neurons with a high level of interconnections.[9] Therefore, memristors, which are made from various materials and operate under different principles, are needed to achieve more faithful emulation of biological systems.

Emerging layered transition-metal dichalcogenides (TMDCs, *e.g.*, $MoS_2$, $WSe_2$, and $WS_2$) are being actively studied as attractive 2D materials for making high-performance nanoelectronic devices.[10−25] Recently, memristive switching behaviors have been observed in a series of electronic devices made from TMDCs and TMDC-derived materials. For example, Sangwan *et al.* reported that gate-tunable memristive transport states can be excited in the back-gated field-effect transistors (FETs) made from polycrystalline single-layer $MoS_2$ structures grown by chemical vapor deposition (CVD), and such recently identified memristive states are attributed to the grain-boundary-mediated migration of sulfur vacancies. This work also implies that only single-layer $MoS_2$ memristors with intersecting grain boundaries exhibit memristive and dynamic negative differential resistance (NDR) characteristics.[25] Bessonov *et al.* demonstrated memristive and memcapacitive devices made from solution-processed $MoO_x/MoS_2$ and $WO_x/WS_2$ heterostructures vertically sandwiched by Ag electrodes, which are similar to the conventional memristor structure consisting of vertically stacked metal/insulator/metal (MIM) layers.[26] Such TMDC-based memristors typically exhibit very low programming voltages in the range of 0.1−0.2 V and abrupt changes in channel resistance during switching courses.[26] Cheng *et al.* experimentally demonstrated memristors based on the 1T phase of exfoliated $MoS_2$ nanosheets, which have a vertically stacked $Ag/MoS_2/Ag$ structure and exhibit an asymmetric $I-V$ characteristic.[27] In comparison with conventional oxide-based memristors, the TMDC-based memristors exhibit relatively lower threshold electric fields ($\sim 10^5$ V/cm) for initiating memristive-switching processes, which is essential for the successful construction and operation of energy-efficient memristor-based neural networks.[25,28] In addition, Sangwan *et al.*'s more recent work implies that a $MoS_2$ memtransistor can be described as a Schottky barrier transistor, in which the Schottky barriers at the contact regions can be dynamically tuned by external biases, therefore resulting in the modulation of the channel conductance.[9] Such a switching scheme distinguishes $MoS_2$ memtransistors from conventional filament-based memristors. More importantly, it could serve as a device platform to realize multiterminal neuromorphic circuits capable of emulating multiple synaptic connections in real biological neurons. Despite such progresses in 2D-material-based memristors, additional device-oriented research is needed to fully understand the switching mechanisms in the memristive devices made from $MoS_2$ and other 2D-layered TMDCs. The ultimate goal of such effort is to make reliable and consistent 2D-material-based memristors suitable for constructing working neural networks. Especially, such memristors are anticipated to be capable of emulating ionic interactions involved in real synaptic processes.

In this article, we present a systematical study on the switching behaviors of mechanically printed few-layer $MoS_2$ memristors. In this work, we identified two types of dc-programmed switching characteristics, termed rectification-mediated and conductance-mediated behaviors, among different $MoS_2$ memristors. These two types of switching behaviors are attributed to modulation of $MoS_2$/metal Schottky barriers and redistribution of vacancies in the $MoS_2$ channel. Furthermore, we also found that an as-fabricated $MoS_2$ memristor initially exhibits an analog switching behavior under modulation of time sequential voltage pulses, whereas, after an electrical stress process, it becomes a quasi-binary memristor with an abrupt switching behavior. Such a transition of pulse-programmed switching characteristics is attributed to field-induced agglomeration of ionic vacancies at $MoS_2$/metal interfaces. The additional Kelvin probe force microscopy (KPFM), Auger electron spectroscopy (AES) analysis, and electronic characterization results strongly support this hypothesis. In addition, we fabricated a testing device consisting of two adjacent $MoS_2$ memristors and experimentally demonstrated that these two memristors can be coupled to each other through manipulating the distribution of vacancies around their common Schottky junction. This device interconnection scheme could be further developed and used for constructing neural networks capable of emulating complicated ionic interactions among neurons.

## RESULTS AND DISCUSSION

Figure 1(a) illustrates the schematic structure of a few-layer $MoS_2$ memristor, which can be made by using our previously

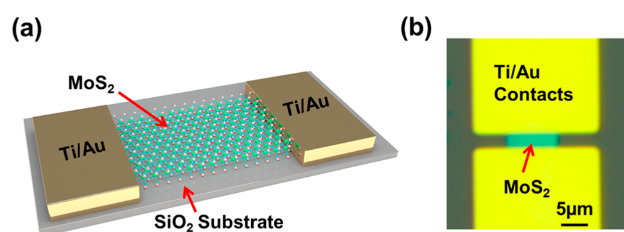


**Figure 1. (a) Schematic illustration of a few-layer $MoS_2$ memristor fabricated by nanoimprint-assisted shear exfoliation (NASE); (b) optical micrograph of a representative memristor with a NASE-produced few-layer $MoS_2$ channel ($MoS_2$ thickness: ∼15 nm, channel length: 2 μm, average channel width: ∼5 μm) and a pair of Ti/Au drain/source contacts (5 nm Ti/50 nm Au).**

reported nanoimprint-assisted shear exfoliation (NASE) method, which is a mechanical nanoprinting lithography technique.[29,30] The detailed information about the device fabrication is described in the Methods and Materials section. Figure 1(b) shows the top-view optical micrograph of a representative few-layer $MoS_2$ memristor. For such a memristor, the $MoS_2$ channel thickness is ∼15 nm, the channel length is 2 μm, and the average channel width is ∼5 μm. In this work, these dimension sizes of the $MoS_2$ channel can be controlled by NASE in combination with photolithography.[29,30] The $MoS_2$ channel is laterally sandwiched by a


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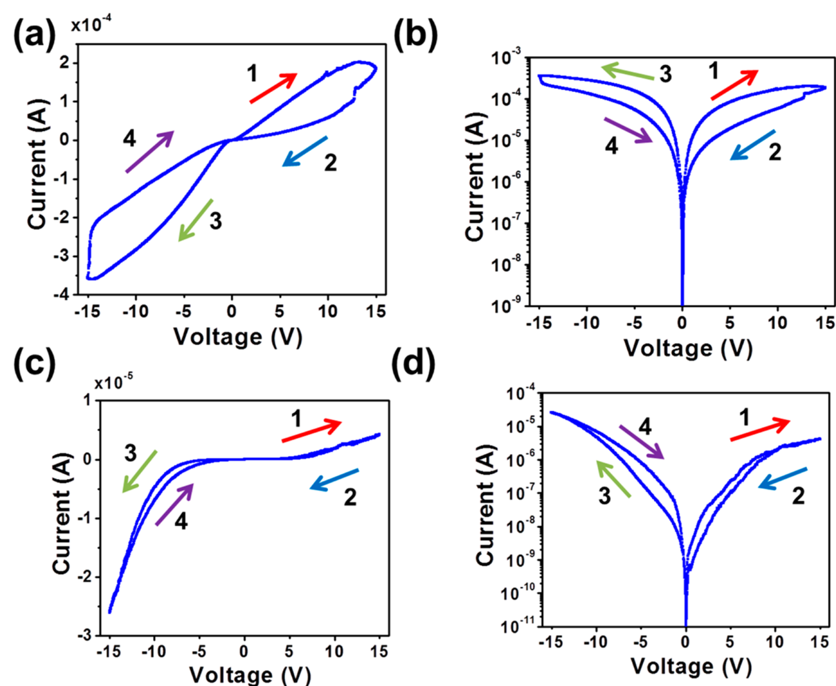


**Figure 2.** Two types of dc-programmed switching characteristics observed from two representative few-layer $MoS_2$ memristors: (a and b) rectification-mediated switching characteristic curve (the same hysteretic *I*−*V* curve plotted in linear and semilogarithmic scales, respectively); (c and d) conductance-mediated switching characteristic curve (the same hysteretic *I*−*V* curve plotted in linear and semilogarithmic scales, respectively). All hysteretic *I*−*V* characteristic curves were acquired with a voltage-sweep rate of 5 V/s, and the directions of four voltage-sweep steps (1−4) in a switching cycle are labeled.

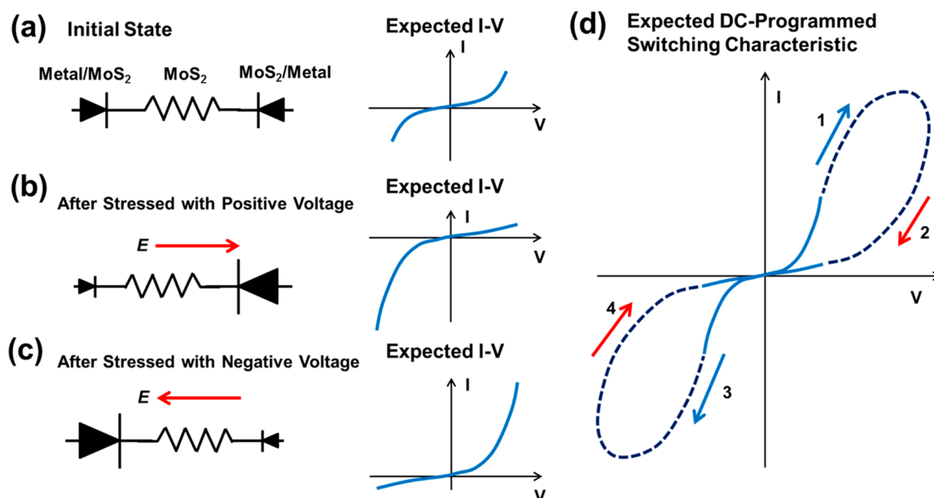


**Figure 3.** Qualitative device model for explaining the rectification-mediated dc-programmed switching process, which involves three memristive states: (a) initial state, (b) backward-diode state, (c) forward-diode state. In this model, a $MoS_2$ memristor is described as a $MoS_2$ channel sandwiched by two metal/$MoS_2$ Schottky diodes with opposite directions. The inset views in (a)−(c) illustrates the expected small-signal *I*−*V* characteristics for corresponding states. (d) Expected dc-programmed switching characteristic curve, in which the solid lines are the small *I*−*V* characteristics for both forward-diode and backward-diode states, and the dashed lines illustrate the switching courses between two states.

pair of Ti (5 nm)/Au (50 nm) electrode contacts. The whole $MoS_2$ memristor is fabricated on a $P^+$-Si substrate with a thermally grown 300 nm thick $SiO_2$ surface layer.

First of all, we studied the resistive-switching characteristics of our $MoS_2$ memristors under modulation of dc voltage and found that two types of dc-programmed switching characteristics are observed among different $MoS_2$ memristors. Specifically, Figure 2 plots examples of these two types of dc-programmed switching characteristics (*i.e.*, hysteretic *I*−*V* characteristic curves) measured from two representative $MoS_2$ memristors, respectively. For both hysteretic *I*−*V* measurements, the voltage-sweep rate is 5 V/s, and the directions of four voltage-sweep processes (1−4) in a measurement cycle are labeled in Figure 2. Specifically, for the memristor shown in Figures 2(a) and (b) (*i.e.*, the same *I*−*V* curve plotted in linear and semilogarithmic scales, respectively), during voltage-sweep processes 1 and 2 (*i.e.*, 0 to 15 V to 0), its conductance gradually decreases. Upon the completion of sweep processes 1


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and 2, the memristor is set to a relatively low-conductance state for the positive-V regime. Afterward, this memristor undergoes sweep process 3 (*i.e.*, 0 to −15 V). In this regime, the memristor exhibits a relatively high-conductance state for the negative-V bias compared with the positive-V bias. The whole sweep processes 3 and 4 (*i.e.*, 0 to −15 V to 0) subsequently decrease the memristor's conductance for the negative-V bias but simultaneously increase its conductance for the positive-V bias, therefore ultimately setting the memristor back to its original electronic state before the measurement cycle. For the memristor shown in Figures 2(c) and (d) (*i.e.*, the same $I-V$ curve plotted in linear and semilogarithmic scales, respectively), voltage-sweep processes 1 and 2 (*i.e.*, 0 to 15 V to 0) also gradually decrease its conductance and therefore set the memristor to a relatively low-conductance state for the positive-V bias. Different from the one shown in Figures 2(a) and (b), when this memristor subsequently undergoes sweep process 3 (*i.e.*, 0 to −15 V), it remains in the relatively low-conductance state for both negative- and positive-V biases. The whole sweep processes 3 and 4 (*i.e.*, 0 to −15 V to 0) subsequently increase the memristor's conductance for both positive- and negative-V biases, therefore setting the memristor back to its original electronic state before the measurement cycle. Both of these two types of dc-programmed resistive-switching behaviors are highly repeatable, and the corresponding hysteretic $I-V$ curves are smooth without exhibiting any abrupt change of conductance. Therefore, such memristors are suitable for analog switching applications.

In terms of the $I-V$ characteristics of two-terminal devices, the switching processes shown in Figure 2(a)/(b) and (c)/(d) can be described as rectification-mediated and conductance-mediated switching behaviors driven by dc bias, respectively. In a rectification-mediated switching process, the applied dc voltage (or electric field) gradually modifies the memristor's degree of rectification, which is defined as the forward/backward conductance (or current) ratio measured at given $\pm V$ (*e.g.*, ±1 V). Specifically, Figure 3 illustrates our qualitative device model for describing such a switching behavior. In this model, a $MoS_2$ memristor is described as a $MoS_2$ channel sandwiched by two metal/$MoS_2$ Schottky diodes with opposite directions, as illustrated in Figure 3(a). In previous works, the work function of Ti is reported to be around 4.3 eV.[31,32] Pristine $MoS_2$ is reported to be an n-type semiconductor with a work function of ~4.6 eV.[33,34] Based on the classical Schottky−Mott rule, $MoS_2$ and Ti are theoretically anticipated to form a nonrectifying contact. However, recent experimental works show that the Schottky barrier height (SBH) at a $MoS_2$/metal contact exhibits a very weak dependence on the work function of the metal, and the $MoS_2$/Ti contact indeed has a relatively high SBH (~0.18 eV).[31,35] Such a weak dependence of the $MoS_2$/metal SBH on the metal work function is attributed to the Fermi level pinning effect, which is also responsible for the formation of rectifying contacts between $MoS_2$ channels and metals with relatively lower work-functions.[31,35,36] For $MoS_2$/metal contacts, Fermi level pinning is mainly attributed to atomic vacancies and structural defects on both $MoS_2$ and metal surfaces.[37,38] We assume that an as-fabricated $MoS_2$ memristor has a symmetric diode/$MoS_2$/diode structure and therefore exhibits a symmetric small-signal $I-V$ characteristic, as sketched in the inset of Figure 3(a). This assumption is quite consistent with our experimental observation. Here, "small-signal $I-V$" is referred to the analytical $I-V$ characteristic acquired within a relatively small voltage range well below the threshold for initiating memristive switching, and it can serve as a transport state property of the memristor to indicate its instant conductance state. When the memristor is biased with a positive voltage higher than the threshold voltage for initiating memristive switching (typically, 10 V for a 2 $\mu$m long $MoS_2$ channel), the resulting electric field (typically, $E > 10^4$ V/cm) induces the drift of sulfur (S) vacancies toward the right electrode. Such field-induced drift of S vacancies and defects has been studied in a series of previous works.[39,40] Especially, in a recently published work, Sangwan *et al.* hypothesize that the defects in $MoS_2$ layers act as dopants and their local migration facilitated by grain boundaries is responsible for the modulation of the Schottky barrier at the $MoS_2$/metal interface.[9] In our specific work, based on our experimental results, we tentatively hypothesize that the S vacancies, when presented in the proximity of a Ti/Au contact, increase the Schottky barrier at the corresponding Ti/$MoS_2$ interface. Therefore, as illustrated in Figure 3(b), the applied positive voltage (or electric field) gradually depletes the S vacancies from the proximity region of the left electrode and accumulates more vacancies around the right electrode. This results in the decrease of the Schottky barrier as well as rectification degree of the left $MoS_2$/metal Schottky diode and simultaneously results in the increase of those of the right diode. In Figure 3(b), the modified rectification degrees of these two Schottky diodes are highlighted by the sizes of their diode symbols. The inset of Figure 3(b) shows the corresponding sketch of the small-signal $I-V$ characteristic. This memristive state is termed as a "backward-diode state". Similarly, Figure 3(c) illustrates the case in which the memristor is biased with a negative voltage that is higher than the threshold voltage for initiating memristive switching. In this case, the rectification degrees of left and right $MoS_2$/metal Schottky diodes are increased and decreased, respectively. The corresponding $I-V$ characteristic is sketched in the inset of Figure 3(c). This state is termed as a "forward-diode state". Based on this device model, the dc-programmed switching characteristic curve can be sketched as shown in Figure 3(d), in which the solid lines are the small $I-V$ characteristics for both forward-diode and backward-diode states, and the dashed lines illustrate the switching courses between these two states. Such a switching behavior derived from this hypothesized model is consistent with the rectification-mediated characteristics experimentally observed in our $MoS_2$ memristors (*e.g.*, the one shown in Figure 2(a)).

The observed conductance-mediated switching behavior (*e.g.*, Figure 2(c) and (d)) is tentatively attributed to a hypothesized situation as follows. During a dc-programmed switching cycle, there are not a significant number of S-vacancies that ever reach the proximity regions of the metal contacts. This is expected to happen when a significant number of S vacancies are blocked or retarded by other crystal defects in the $MoS_2$ channel, therefore resulting in relatively low field-effect mobilities or high diffusion barriers for S-vacancies. In such a case, the applied dc bias can hardly modulate the Schottky barriers at $MoS_2$/metal interfaces, and the observed resistive-switching behavior is mainly attributed to the field-induced redistribution of S vacancies or other movable defects. The channel conductance associated with a memristive state is also expected to exhibit a very weak dependence on the bias polarity. Such a hypothesized scenario can explain the conductance-mediated switching characteristics shown in



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Figure 2(c) and (d). The $I-V$ curves shown in Figure 2(c) and (d) are smooth and do not exhibit any abrupt changes in current. This implies that the conductance-mediated switching process in a $MoS_2$ memristor does not involve the formation and rupture of a complete conductive filament between electrodes.

Upon the basis of this hypothesized scheme, we further speculate that, for a $MoS_2$ memristor exhibiting the conductance-mediated switching behavior under the regular voltage-sweep condition (*i.e.*, the condition shown in Figure 2), a larger sweep range of dc voltage could greatly enhance the average mobility of S vacancies during a switching cycle and ultimately let a significant number of S vacancies reach the proximity regions of the Schottky barriers. If this happens, the memristor is anticipated to exhibit a transition from the conductance-mediated switching mode to the rectification-mediated one through increasing the voltage-sweep range. To support this implication, we further measured the dc-programmed switching characteristics of a $MoS_2$ memristor under different voltage-sweep ranges, as plotted in Figure 4.

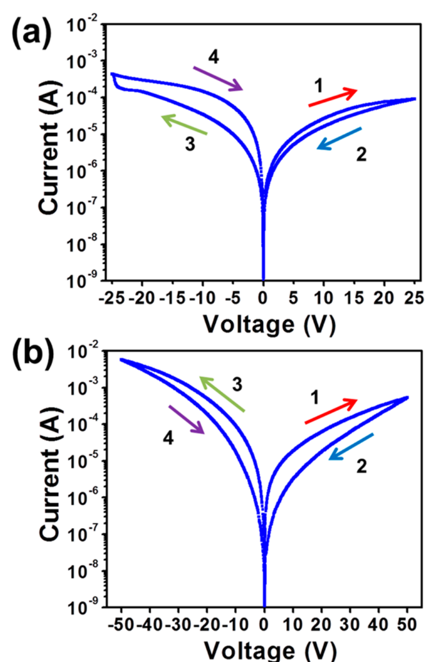


**Figure 4. Two different dc-programmed switching characteristics measured from a single $MoS_2$ memristor: (a) conductance-mediated switching characteristic measured in the voltage-sweep range of −25 to 25 V and (b) rectification-mediated switching characteristic observed in the voltage-sweep range of −50 to 50 V. All $I-V$ characteristic curves were acquired with a voltage-sweep rate of 5 V/s.**

Under a relatively smaller voltage-sweep range (*i.e.*, −25 to 25 V), this selected memristor exhibits a conductance-mediated switching behavior (Figure 4(a)), whereas when the voltage-sweep range is extended to 50 to −50 V, it becomes a rectification-mediated one (Figure 4(b)). This experimental result highly supports our hypothesized scheme for explaining the observed conductance-mediated and rectification-mediated memristive-switching characteristics.

To construct reliable neural networks, it is needed to develop fabrication routes that can produce $MoS_2$ memristors with deterministic switching characteristics. In this work, we further identified a practical fabrication condition, under which $MoS_2$ memristors with rectification-mediated switching characteristics can be reliably produced, whereas the generation of conductance-mediated memristors can be effectively inhibited. As we discussed above, the observed conductance-mediated switching behavior is tentatively attributed to the limited number of S-vacancies that ever reach the proximity regions of metal contacts. Our hypothesis also implies that this situation could be effectively mitigated by reducing the memristor channel length. In a relatively shorter memristor channel, a larger number of S-vacancies are expected to reach the proximity regions of $MoS_2$/metal interfaces during a dc-programmed switching cycle. Motivated by this implication, we also fabricated and characterized a bunch of memristors with a relatively shorter channel length (*i.e.*, 1 $\mu$m long memristors in comparison with aforementioned 2 $\mu$m long memristors). Figure S1 in the Supporting Information displays the dc-programmed switching characteristics of 10 1-$\mu$m-long $MoS_2$ memristors fabricated under the same condition. All of these memristors exhibit a rectification-mediated switching behavior. Here, it should be noted that the conductance-mediated switching behavior should be avoided in the construction of a neural network based on $MoS_2$ memristors. This is because such a switching scheme associated with the redistribution of S-vacancies is not expected to result in a prominent change of the Schottky barriers at $MoS_2$/Ti interfaces, and it can only result in a minor switching ratio, as demonstrated in Figure 2(c) and (d). Currently, we still lack an effective method to enhance the switching ratios of conductance-mediated memristors.

The pulse-programmed switching characteristics of memristive devices are critical for analog computing and synaptic applications. Figure 5 displays the pulse-programmed switching

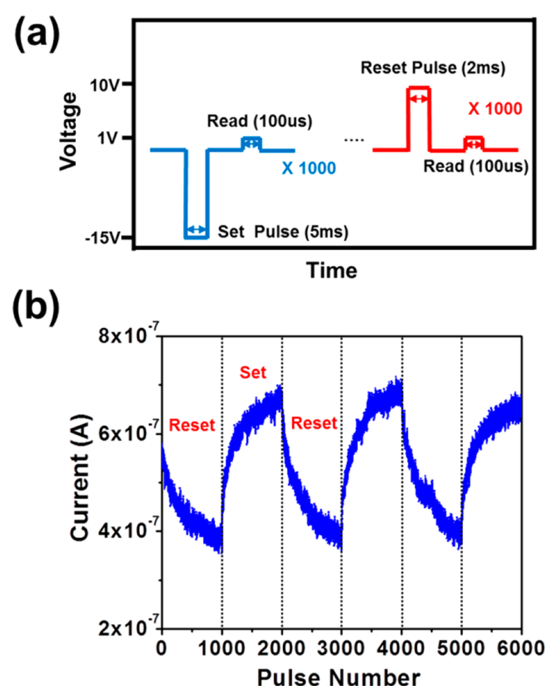


**Figure 5. Analog pulse-programmed switching characteristics of a representative few-layer $MoS_2$ memristor: (a) signal profiles of voltage pulses for gradually switching the conductance state of the memristor; (b) measured current *versus* pulse number ($I-n$) curve that involves three switching cycles.**



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characteristics measured from one of our representative $MoS_2$ memristors. Specifically, Figure 5(a) sketches the profiles of voltage pulses applied for switching the memristor. During a switching cycle, a train of 1000 −15 V, 5 ms set pulses are applied to gradually increase the device conductance (or the channel current ($I$) measured under a fixed sampling voltage of 1 V), and a subsequent train of 1000 +10 V, 2 ms reset pulses are applied to gradually decrease the device conductance. Following each set or reset pulse, the instant channel current ($I$) is measured under a fixed +1 V, 0.1 ms read pulse. Figure 5(b) plots the measured channel current ($I$) *versus* pulse number ($n$) curve that involves multiple switching cycles. Such an $I$−$n$ characteristic curve shows that the $MoS_2$ memristor under study exhibits an analog pulse-programmed switching behavior; that is, both set and reset courses exhibit a gradual modulation of the device conductance. Our other $MoS_2$ memristors fabricated under the same processing condition exhibit very similar and consistent analog switching characteristics.

It should be noted that for most of our $MoS_2$ memristors the set and reset pulse durations are in a constant ratio of 5:2, with which the pulse number for gradually setting the memristor to a higher conductance state and the required pulse number for subsequently recovering the memristor back to the original state are equal. For example, Figure 6 displays the pulse-programmed switching characteristics of a single $MoS_2$ memristor, which were measured with different set/reset pulse durations but at a constant ratio of set/reset pulse durations (*i.e.*, (a) 20 ms/8 ms, (b) 10 ms/4 ms, (c) 5 ms/2 ms, (d) 0.5 ms/0.2 ms). For all cases, the numbers of set and reset pulses remain the same. Such a linearity between set and reset pulse durations is important for practical neuromorphic and analog computing applications, especially in the case in which the durations of programming pulses are used to linearly represent the input signals for a neural network.

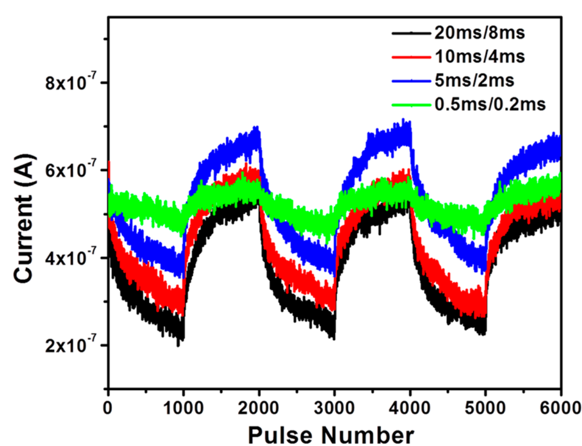


**Figure 6. Pulse-programmed switching characteristics measured from a single $MoS_2$ memristor, which were acquired under different set/rest pulse durations: 20 ms/8 ms (black), 10 ms/4 ms (red), 5 ms/2 ms (blue), 0.5 ms/0.2 ms (green). For all measurements, set and reset pulse amplitudes are −15 and +10 V, respectively.**

All our as-fabricated $MoS_2$ memristors exhibit very stable and consistent analog pulse/dc-programmed switching characteristics if the programming voltage is lower than 20 V (the corresponding field magnitude is ∼$10^5$ V/cm). However, we found that the repetitive application of a voltage higher than 20 V can modify the switching mode of a $MoS_2$ memristor from the analog mode to the discrete mode. Specifically, Figure 7(a)

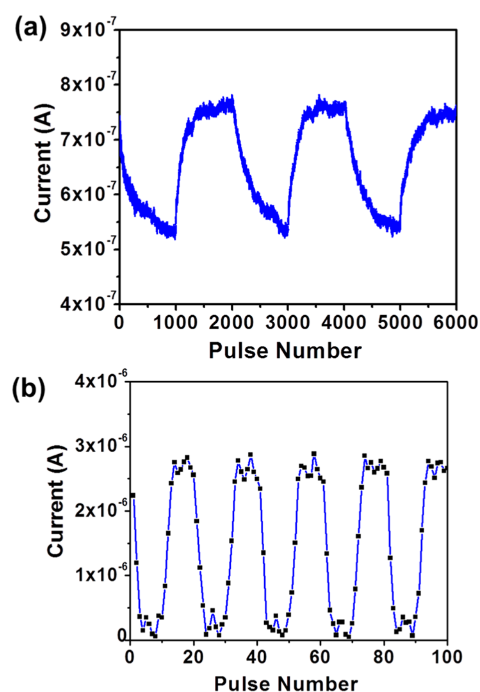


**Figure 7. Two different pulse-programmed switching characteristics measured from a single few-layer $MoS_2$ memristor: (a) analog and (b) discrete switching characteristics, respectively.**

shows the pulse-programmed switching characteristic curve (or $I$−$n$ curve) measured from a representative as-fabricated $MoS_2$ memristor (the measurement condition is the same as that for Figure 5). It shows that this memristor was initially in the analog switching mode. After this measurement, this memristor was subjected to a designated electrical stress that included three consecutive voltage sweeps (in each sweep, voltage was swept from 0 to 50 V and then back to 0 V; the sweep rate was 5 V/s). After this electric stress, the $I$−$n$ switching curve of this memristor was remeasured and plotted in Figure 7(b) (set process: 10−12 V, 50 ns pulses; reset process: 10 + 12 V, 50 ns pulses). Figure 7(b) indicates that the switching mode of this memristor has been modified to a discrete (or quasi-binary) mode. In such a discrete switching mode, the memristor exhibits only two metastable conductance states, and the transition between these two states occurs during the fast-transient process for switching the polarity of applied voltage pulses. We also remeasured the $I$−$n$ switching curve of the memristor shown in Figure 7(b) using a set of different programming pulse trains (*i.e.*, set process: 20 −12 V, 250 ns pulses; reset process: 20 +12 V, 250 ns pulses). Figure S2 in the Supporting Information displays the remeasured $I$−$n$ curve. This curve further shows that a single set/reset pulse with a duration of 250 ns can directly switch the memristor between highest and lowest conductance metastable states. Therefore, the switching time of such a discrete memristor is estimated to be about 250 ns. Our further tests verified that other types of high electrical stress (*e.g.*, a sequential train of 5000 20 V, 2 ms pulses or 20 V dc bias for more than 20 s) can also modify a $MoS_2$ memristor's switching characteristic from the analog mode to the discrete mode, and this transition phenomenon is a generic device character for all $MoS_2$ memristors. Such a


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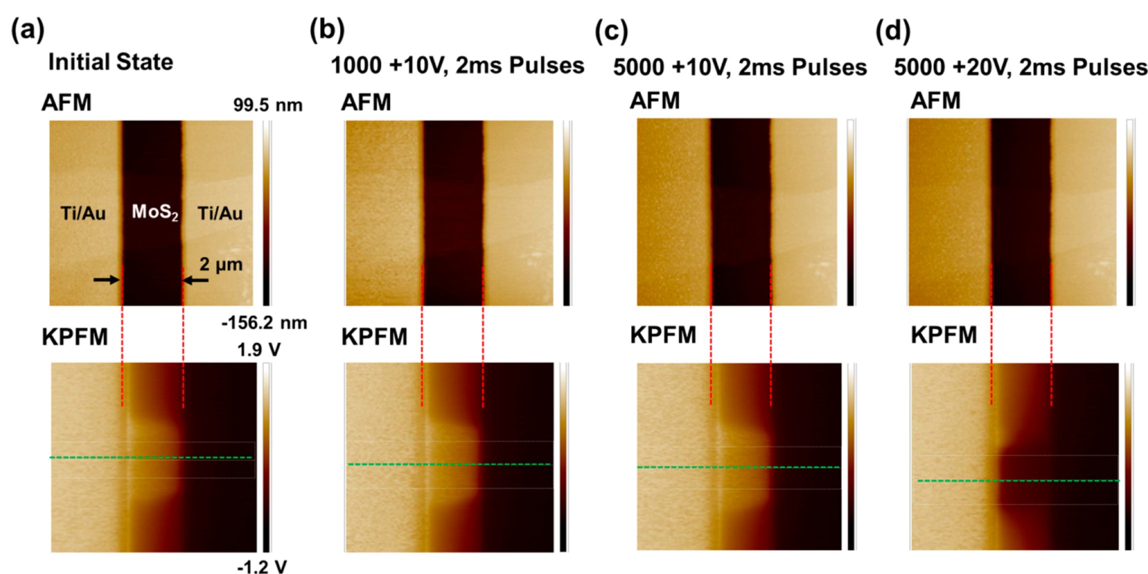


Figure 8. AFM and corresponding KPFM images measured from a representative $MoS_2$ memristor, which was programmed to various memristive states by using a set of voltage pulse signals: (a) initial state, (b) 1000 +10 V, 2 ms pulses, (c) 5000 + 10 V, 2 ms pulses, (d) 5000 +20 V, 2 ms pulses. During the KPFM characterization, the memristor is under a dc bias of +3 V.

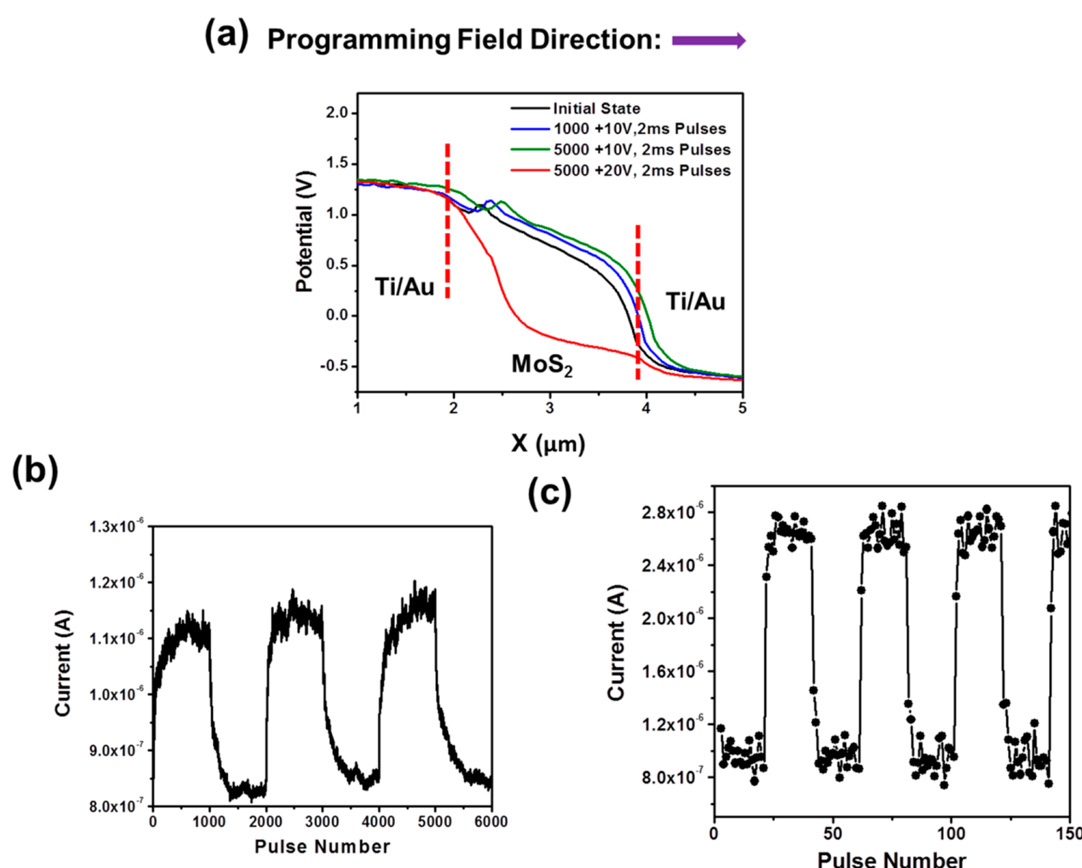


Figure 9. (a) Potential distribution profiles captured from the KPFM images shown in Figure 8, in which the red dashed lines denote the locations of the $MoS_2$/Ti interfaces. Plot the pulse-programmed switching characteristic curves ($I$−$n$ curves) of the memristor measured (b) before and (c) after the application of 5000 +20 V, 2 ms voltage pulses, respectively.

character is expected to be critical for making reliable synaptic devices based on $MoS_2$ memristors in the future and should be further studied. In addition, this character, if fully understood, could provide additional information for making biorealistic synaptic devices with variable transport properties.

To explore the mesoscopic mechanisms responsible for the observed memristive-switching characteristics as well as the transition between different switching modes, we performed a Kelvin probe force microscopy analysis on $MoS_2$ memristors. The detailed information about the KPFM measurement is


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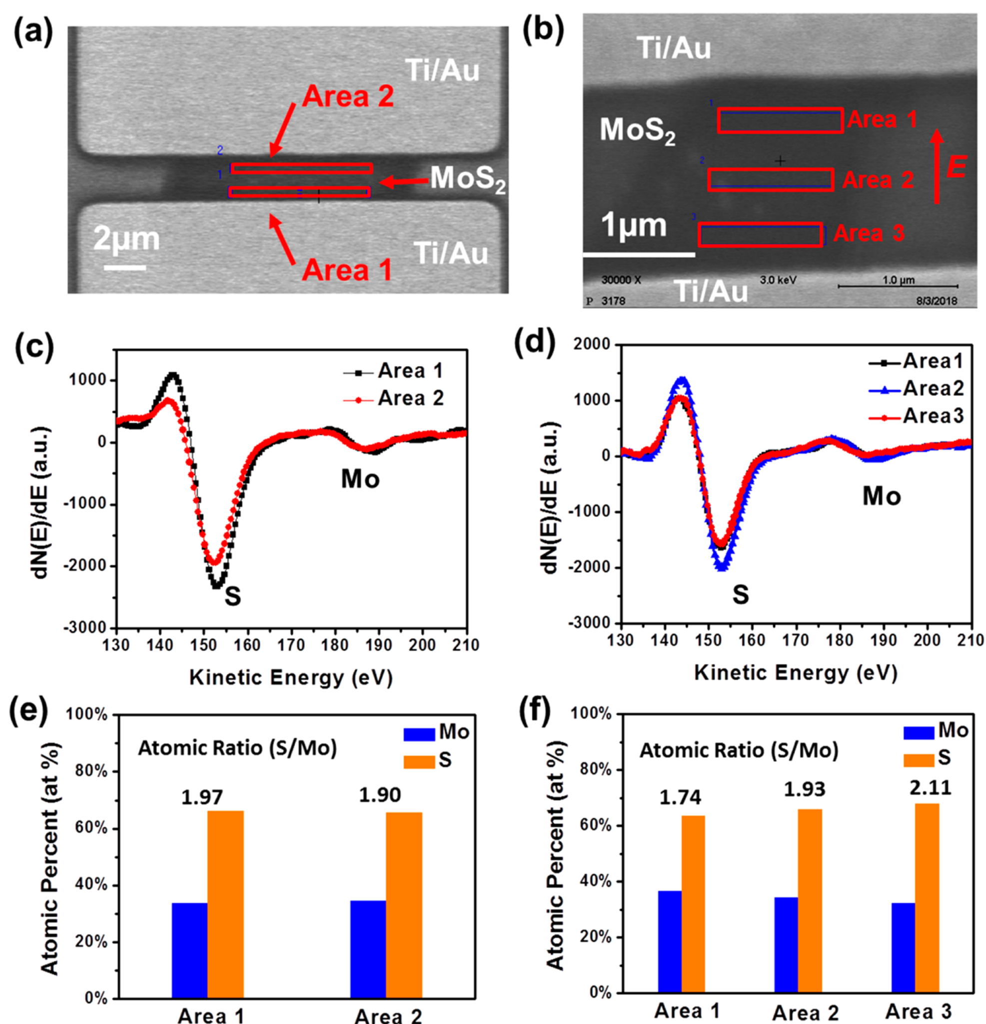


**Figure 10. Auger electron spectroscopy (AES) analysis: (a, b) SEM images of the intact control $MoS_2$ memristor and the electrically treated one, respectively, in which the red boxes denote the AES sampling areas, and the red arrow in (b) indicates the electric field direction of applied pulses; (c, d) differential energy distribution spectra of Auger electrons captured from the sampling areas in control and electrically treated memristors, respectively; (e, f) atomic percent values of Mo/S atoms within the sampling areas in control and electrically treated memristors, respectively.**

described in the Methods and Materials section. Figure 8 displays the KPFM images measured from a representative $MoS_2$ memristor. In this measurement, this memristor was programmed to various memristive states by using a set of voltage pulse signals (*i.e.*, (a) initial state, (b) 1000 +10 V, 2 ms pulses, (c) 5000 +10 V, 2 ms pulses, (d) 5000 +20 V, 2 ms pulses, as listed in Figure 8). At each state, the KPFM image and the corresponding atomic force micrograph (AFM) are captured together. The KPFM image shows the potential distribution over the entire $MoS_2$ channel under a dc bias of +3 V. The corresponding AFM image is used to specify the locations of $MoS_2$/Ti interfaces, as indicated by the red dashed lines in Figure 8. To analyze the evolution of the potential distribution over the $MoS_2$ channel at various states, the potential profiles for these states are extracted from the center lines of corresponding KPFM images (indicated by the green dashed lines in Figure 8) and plotted in Figure 9(a). The red dashed lines in Figure 9(a) denote the locations of $MoS_2$/Ti interfaces. Figure 9(a) shows that with increasing the number of the applied +10 V, 2 ms voltage pulses, the $MoS_2$/Ti Schottky barrier, to which the programming pulse field points (*i.e.*, the right barrier), gradually increases, while the barrier on the other side decreases. Such a KPFM result supports our diode/$MoS_2$/diode model (in Figure 3) for explaining the analog dc- and pulse-programmed switching characteristics measured from our $MoS_2$ memristors.

Figure 9(a) also indicates that when this memristor was applied with a relatively high electric stress (*i.e.*, a train of 5000 +20 V, 2 ms voltage pulses), the potential distribution over the $MoS_2$ channel undergoes an abrupt change. We found that this abrupt change of the potential distribution happens together with the transition of the switching mode. More specifically, Figure 9(b) plots the pulse-programmed switching characteristic curve ($I$−$n$ curve) of the memristor measured before the application of 5000 +20 V, 2 ms voltage pulses, which exhibits an analog switching behavior. However, after the application of 5000 +20 V, 2 ms pulses, the remeasured $I$−$n$ curve exhibits a rapid discrete switching mode, as shown in Figure 9(c). The combination of the results shown in Figure 9(a) and (c) indicates that when a $MoS_2$ memristor changes from the analog switching mode to the discrete switching mode, the dc potential drops across its Schottky barriers exhibit an abrupt change. Such an experimental correlation between the abrupt change of Schottky barriers and the switching mode transition


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is consistent with the implication that the observed switching mode transition could be reasonably attributed to the electrical-stress-induced agglomeration of S vacancies (or formation of large vacancy clusters) at $MoS_2$/Ti interfaces.

To further support the implication from our electrical and KPFM characterizations, we also performed Auger electron spectroscopy analysis to directly track the spatial migration of S vacancies in $MoS_2$ channels. AES is a highly surface-sensitive characterization technique based on analysis of the energetic electrons emitted from an excited atom after a series of internal relaxation events with a single-core hole in the initial state and two holes in the final state.[41] A specific Auger transition is usually denoted by the X-ray notation for the three levels involved. For example, a Mo *MVV* Auger transition means that an electron was first removed from the M level of a Mo atom and then an electron from the V orbital falls to fill the hole at the M orbital. During this process, the released energy excites another valence band electron out of the atom (*i.e.*, an emitted Auger electron), leaving two holes on the V shell in the final state. The energy position and shape of an Auger spectrum peak directly reflect the chemical environment of the target atoms. Typically, the first-order derivatives of Auger spectra are employed to highlight the chemical changes of the target sample.

In our AES analysis, two memristors fabricated under the same condition were chosen for this test. One memristor was electrically treated with a sequential train of 5000 20 V, 2 ms pulses, while the other memristor remained intact and served as a control device. Figure 10(a) and (b) display the SEM images of the control memristor and the electrically treated one, respectively. The red boxes denote a set of chosen AES sampling areas along $MoS_2$ channels. The red arrow in Figure 10(b) indicates the electric field direction of the pulses applied to the electrically treated memristor. The derivative mode AES analysis was performed within the sampling areas in control and electrically treated memristors, and their Auger spectra were plotted in Figure 10(c) and (d), respectively. Figure S4 in the Supporting Information displays these spectra plotted with a full energy range (95−250 eV). For both memristors, the AES features around 153 eV are attributed to S *LVV* Auger transitions.[42] For the electrically treated memristor, the energy positions of S *LVV* features measured from different sampling areas are nearly the same. However, the energy positions of Mo *MVV* features from these areas exhibit a prominent variation along the direction of applied electric field (*i.e.*, 188.3 eV for area 1; 186.9 eV for area 2; 186.2 eV for area 3). Table S1 in the Supporting Information lists the detailed energy positions of the S *LVV* and Mo *MVV* transitions measured from different AES sampling areas. If the S *LVV* transition features measured from different areas are shifted to the same position (153 eV), the calibrated energy positions of Mo *MVV* features from these areas exhibit a more prominent spatial variation (*i.e.*, 188.5 eV for area 1; 187.0 eV for area 2; 186.0 eV for area 3), as indicated by the Mo (calibrated) column in Table S1. Such a spatial variation of Mo *MVV* features indicates that the applied electric field has altered the chemical states of the Mo atoms along the channel.[43] The lower kinetic energy of Auger electrons from Mo atoms suggests a higher binding energy of Auger electrons from the valence band, since the kinetic energy of Auger electrons can be calculated from the energy released from the two-inner-shell transition minus the binding energy of the Auger electron level, while the inner energy levels are much less affected by the chemical states. A similar observation has been reported for the preferentially sputtered $MoS_x$, where the (Mo $3d_{5/2}$ − S $2p_{3/2}$) binding energy gap nearly linearly increases with the $MoS_x$ stoichiometry.[43]

From such Auger spectra, the chemical compositions within the sampling areas can be extracted since the peak-to-valley height of a first-order derivative AES feature is proportional to the product of the elemental concentration and its sensitivity factor.[44−46] The detailed information about the chemical composition calculation is described in the Supporting Information. Figure 10(e) and (f) show the atomic percentages of Mo/S atoms within the sampling areas in control and electrically treated memristors, respectively. For the intact control memristor, the S/Mo ratios measured from two sampling areas are very close to 2 (*i.e.*, 1.97 for area 1; 1.90 for area 2), which is consistent with the stoichiometry of pristine $MoS_2$. However, for the electrically treated memristor, the S/Mo atomic ratios measured from three sampling areas exhibit a clear gradient distribution along the electric field direction of the applied pulses (*i.e.*, 1.74 for area 1; 1.93 for area 2; 2.11 for area 3). This indicates that a significant number of S vacancies have migrated toward the electrode that the treating electric field is pointing to. This result further supports the implications from aforementioned electrical and KPFM characterizations. In addition, we also performed a Monte Carlo computation to simulate the kinetic behaviors of S vacancies in a $MoS_2$ memristor channel. The detailed information about this model is described in the Supporting Information.

To further support our conclusion that the large vacancy clusters are the critical factors responsible for the observed discrete switching mode, we tested using another method rather than electrical stress to generate large vacancy clusters at $MoS_2$/Ti interfaces and verified if such vacancy clusters could also result in a discrete memristive switching behavior for the tested $MoS_2$ memristor. Our previous works indicate that plasma treatment can introduce high concentration ionic defects/vacancies within a designated $MoS_2$ surface area.[47,48] In this work, we used an energetic $O_2$ plasma treatment process to introduce high-concentration vacancies within the contact areas of a $MoS_2$ memristor channel before the deposition of Ti/Au electrodes. The rest of the $MoS_2$ channel remained untreated. The details about plasma treatment are described in the Methods and Materials section. Figure 11 plots the pulse-programmed switching characteristic curve (*I*−*n* curve) measured from the tested memristor (measurement

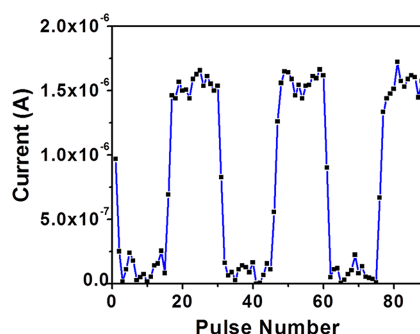


**Figure 11. Pulse-programmed switching characteristic curve (*I*−*n* curve) measured from a plasma-treated memristor. Measurement cycle conditions: a train of 15 +12 V, 50 ns set pulses for increasing the device conductance followed by a train of 15 −12 V, 50 ns reset pulses for decreasing the conductance.**


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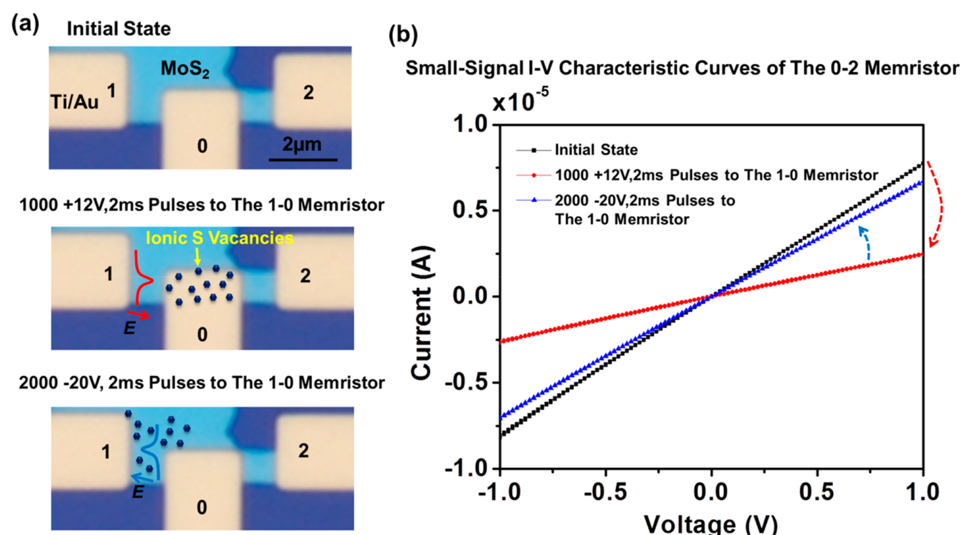


**Figure 12. Demonstration of a testing device consisting of two adjacent $MoS_2$ memristors, which can be coupled to each other: (a) optical micrograph of the testing device, in which a few-layer $MoS_2$ flake is in contact with three Ti/Au electrodes labeled with "0", "1", and "2", and forms two memristors (*i.e.*, 1−0 and 0−2 memristors), as well as illustration of the course for operating the testing device; (b) small-signal *I*−*V* curves measured from the 0−2 memristor at its initial state (black curve), after application of 1000 +12 V, 2 ms pulses to the 1−0 memristor (red curve), and after application of 2000 −20 V, 2 ms pulses to the 1−0 memristor (blue curve).**

cycle condition: a train of 15 +12 V, 50 ns set pulses for increasing the device conductance followed by a train of 15 −12 V, 50 ns reset pulses for decreasing the conductance). This *I*−*n* characteristic curve clearly shows that a $MoS_2$ memristor with plasma-treated $MoS_2$/Ti interfaces directly exhibits a rapid discrete switching behavior. Here, it should be noted that $O_2$ plasma treatment could also form oxygenic groups such as Mo−O and S−O bonds in $MoS_2$ layers.[47−50] In the present work, we cannot completely exclude the contribution of such O dopants to the observed discrete switching characteristics. To further clarify the role of S vacancies in making discrete $MoS_2$ memristors, we also tested using Ar plasma treatment to create discrete $MoS_2$ memristors. Here, Ar plasma treatment is expected to generate high-concentration S vacancies (or large vacancy clusters) in $MoS_2$ layers but hardly introduce other types of dopants.[49] The details about Ar plasma treatment are described in the Methods and Materials section. Figure S3 shows the pulse-programmed switching characteristic curve (*I*−*n* curve) measured from an Ar plasma-treated memristor, which also exhibits a discrete switching behavior. This result further supports our conclusion that the vacancies aggregated at $MoS_2$/Ti interfaces are mainly responsible for the rapid discrete switching mode observed in electrically stressed $MoS_2$ memristors. For typical synaptic device applications, $MoS_2$ memristors need to operate in the analog switching mode. Therefore, the programming signals (*i.e.*, dc or voltage pulse signals) must be limited so that the resulting electrical stress on a $MoS_2$ memristor during a set or reset course does not surpass the critical stress that induces the analog-to-discrete mode transition. This critical stress is expected to be dependent on multiple parameters, such as device dimensions, programming modes, and programming signal profiles. In our work, it is experimentally estimated to be equivalent to the stress on a 2 $\mu$m long $MoS_2$ memristor caused by a sequential train of 5000 20 V, 2 ms pulses, a 20 V dc bias for more than 20 s, or a voltage sweep from 0 to 50 V and then back to 0 V at a sweep rate of 5 V/s.

As discussed above, our $MoS_2$ memristors exhibit two types of transitions of memristive switching characteristics. One type is for dc-programmed switching, and the other type is for pulse-programmed switching. The transition of dc-programmed switching characteristics from the conductance-mediated mode to the rectification-mediated one is attributed to the increase of the number of S vacancies that reach the proximity regions of the Schottky barriers during a dc-programmed switching cycle. As demonstrated in Figure 4, such a transition can be induced by directly increasing the sweep range of dc voltage (*i.e.*, ±50 V for 2 $\mu$m long memristors). Figure 4(b) also shows that during such a transition the corresponding hysteretic *I*−*V* curve is still smooth without exhibiting any abrupt change of conductance. This indicates that such a transition does not necessarily create discrete memristive states in an initially analog memristor. However, the transition of pulse-programmed switching characteristics from the analog mode to the discrete one is attributed to the agglomeration of S vacancies at $MoS_2$/metal interfaces. As demonstrated in Figure 7, such a transition is attributed to the repetitive or long-time application of electrical stress on an initially analog memristor (*i.e.*, three consecutive 0−50 V sweeps, a sequential train of 5000 20 V, 2 ms pulses, or 20 V dc bias for more than 20 s). In principle, these two types of transitions are not directly corrected.

Finally, to preliminarily demonstrate that $MoS_2$ memristors could be used for emulating the synaptic interactions, we fabricated a testing device consisting of two adjacent $MoS_2$ memristors and experimentally demonstrated that these two memristors can affect each other; that is, the programming signal applied to one memristor can modulate the conductance state of the other memristor through the Schottky junction between these two memristors. Recently, Sangwan *et al.* demonstrated a six-terminal memtransistor, in which the conductance state between any two of the four inner electrodes can be modulated by the programming pulses applied to the two outer electrodes.[9] In this previously reported device, only the modulation of conductance states between the inner



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electrodes was achieved. However, in our work, two adjacent memristors can still be coupled. Specifically, Figure 12(a) shows the optical micrograph of this testing device, in which a few-layer $MoS_2$ flake is in contact with three Ti/Au electrodes labeled with "0", "1", and "2", and this structure forms two memristors. Here, the memristor between electrodes "1" and "0" is referred to as the 1−0 memristor, and the memristor between electrodes "0" and "2" is referred to as the 0−2 memristor. Figure 12(a) also illustrates the operation course for this testing device. First, the small-signal $I-V$ characteristic curve of the 0−2 memristor at the initial state was measured and plotted in Figure 12(b) (black curve). Afterward, a train of 1000 +12 V, 2 ms voltage pulses was applied to the 1−0 memristor, and the $I-V$ curve of the 0−2 memristor was subsequently remeasured and plotted in Figure 12(b) (red curve). It was noted that the conductance of the 0−2 memristor prominently decreased after this operation, although there was no programming signal directly applied to the 0−2 memristor. As illustrated in Figure 12(a), the drop of conductance for the 0−2 memristor was attributed to the accumulation of S vacancies around electrode "0", which was induced by the positive programming pulses applied to the 1−0 memristor. Based on our aforementioned analysis and discussion, it was reasonably expected that these accumulated vacancies increased the $MoS_2$/Ti Schottky barrier at electrode "0" and therefore led to a conductance drop for the 0−2 memristor. After this setting operation, another train of 2000 −20 V, 2 ms pulses was applied to the 1−0 memristor, and the corresponding small-signal $I-V$ characteristic curve of the 0−2 memristor was measured again and plotted in Figure 12(b) (blue curve). During this operation, the negative programming pulses applied to the 1−0 memristor largely recovered the conductance of the 0−2 memristor back to its initial state. This observation was attributed to the depletion of S vacancies from the proximity area of electrode "0", which was induced by the negative programming pulses applied to the 1−0 memristor and led to a decrease of the $MoS_2$/Ti Schottky barrier at electrode "0", as illustrated in Figure 12(a). This experiment shows that two $MoS_2$ memristors can be ionically coupled to each other through controlling the spatial distribution of S vacancies around their common Schottky junction. The integration of more such memristors could enable the emulation of the complicated ionic interactions among neurons, which is anticipated to be a promising pathway toward realizing biorealistic neural networks.

## CONCLUSION

In this work, we systematically investigated the switching characteristics of mechanically printed few-layer $MoS_2$ memristors with a lateral device structure. Specifically, we experimentally identified two types of dc-programmed switching modes in such memristors, *i.e.*, rectification-mediated and conductance-mediated modes, which were attributed to modulation of $MoS_2$/Ti Schottky barriers and redistribution of ionic vacancies in the $MoS_2$ channels, respectively. We further found that an as-fabricated $MoS_2$ memristor initially exhibits an analog pulse-programmed switching behavior under modulation of time sequential voltage pulses, whereas, after subjected to an electrical stress process, it becomes a quasi-binary memristors with an abrupt switching character. This transition of switching characteristics is attributed to field-induced agglomeration of ionic vacancies at $MoS_2$/Ti interfaces. The additional KPFM, AES analysis, and electronic characterization results strongly support this hypothesized explanation. Finally, we constructed a testing device consisting of two adjacent $MoS_2$ memristors and experimentally demonstrated that these two memristors can be ionically coupled to each other through manipulating the spatial distribution of S vacancies around their common Schottky junction. This work has advanced the device physics for describing the memristive switching behaviors in 2D-material-based electronic devices and also provided a promising pathway for ultimately realizing biorealistic neuromorphic computing systems based on 2D layered materials.

## METHODS AND MATERIALS

**Fabrication of Few-Layer $MoS_2$ Channels.** The few-layer $MoS_2$ memristor channels are fabricated by using the mechanical printing approach previously reported by us.[29] Specifically, a prefabricated bulk $MoS_2$ stamp with protrusive few-layer mesa arrays is fabricated by using photolithography followed by plasma etching. Here, the natural bulk $MoS_2$ ingot is purchased from SPI, Inc. Afterward, the target substrate is spin-coated with a polymeric fixing layer (*e.g.*, thermoplastics or cross-linkable polymers), and the $MoS_2$ stamp is pressed into the fixing layer through a nanoimprint lithography (NIL) process. After the NIL process, a lab-made motorized roller is used to apply shear stress and displacement between the $MoS_2$ stamp and the substrate. This shear stress/displacement can exfoliate the imprinted few-layer $MoS_2$ mesas onto the substrate. The few-layer $MoS_2$ flakes chosen for fabricating memristors are subsequently located after the removal of the polymeric fixing layer. In this fabrication process, $MoS_2$ channel thicknesses are specifically controlled to be in the range of 10−15 nm, aiming to achieve a high device-to-device consistency as well as expecting a relatively high diffusion coefficient for ionic sulfur vacancies in the $MoS_2$ layers covered by the metal contacts.

**Injection of Vacancy Clusters at the $MoS_2$/Ti Interfaces in a Few-Layer $MoS_2$ Memristor through Plasma Treatment.** Before the Ti/Au contact deposition, the contact areas of a $MoS_2$ memristor channel are exposed to $O_2$ or Ar plasma, while the rest of the $MoS_2$ channel is protected by a photolithography-patterned photoresist and remains untreated. The $O_2$ plasma treatment process is performed in a reactive ion etching (RIE) tool (YES-CV200RFS(E)). The RF power is set to 100 W, the chamber pressure is 10 mTorr, the $O_2$ flow rate is 35 sccm, and the processing time is 10 s. The Ar plasma treatment process is performed in a RIE tool (Plasmatherm 790). The RF power is set to 200 W, the chamber pressure is 30 mTorr, the Ar flow rate is 35 sccm, and the processing time is 300 s.

**Electrical Characterizations of Few-Layer $MoS_2$ Memristors.** All electrical characterizations are performed by using a Keithley 4200A-SCS parameter analyzer equipped with two ultrafast $I-V$ modules (model: 4225-PMU). During the characterization of a $MoS_2$ memristor, the Si substrate of this memristor is floating. Our previous works on $MoS_2$ and $WSe_2$ transistor memories indicate that the defects (or charge traps) in the $SiO_2$ layer of a $MoS_2$ memristor can result in a change of the conductance of the $MoS_2$ channel in the case in which a variable electric field vertically penetrates through the $SiO_2$ layer and induces the charging/discharging processes associated with such defects.[51,52] In this work, since the $Si/SiO_2$ substrate is floating during the measurement, the defects in the $SiO_2$ layer are expected to result in a negligible effect on the memristive switching characteristics of the $MoS_2$ memristor.

**Surface Characterizations of Few-Layer $MoS_2$ Memristors.** AFM and KPFM imaging processes are performed in a Bruker ICON AFM system. All AFM and KPFM images are acquired in the electrical and magnetic lifting modes using SCM-PIT-V2 tips (Bruker Inc.). The tip radius is ∼25 nm, and the resonant frequency of the tip is 75 kHz. During a KPFM imaging process, the tip cantilever maintains a tip−surface distance of ∼50 nm to avoid damage to the memristor structures, and the memristor under study is biased with a dc voltage of 3 V.


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**Auger Electron Spectroscopy Analysis.** The Auger spectroscopy data were collected on a PHI 680 Auger nanoprobe that is equipped with a field emission electron gun and a cylindrical mirror energy analyzer (energy resolution $\Delta E/E \approx 0.25\%$). The base pressure of the test chamber is around $1.2 \times 10^{-9}$ Torr. To avoid the charging effect of insulating samples under electron beam irradiation, the devices were placed on a tilt stage to reduce the embedded charging effect caused by the deep penetration of the incident electron beam, and a small electron beam current of 1 nA with an acceleration voltage of 3 kV was used to irradiate the specimens. The kinetic energies of Auger electrons were calibrated using the sulfur Auger peak at 153 eV. The quantitative analysis was performed using sensitive factors derived from a pristine $MoS_2$ standard (natural $MoS_2$ bulk ingot), which was measured under the same conditions on the samples to cancel the correction factors associated with the setup particularities.

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.8b03977.

Additional figures and tables (PDF)

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### Notes

The authors declare no competing financial interest.

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